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The Effects and Reduction of Common-Mode Noise and Electromagnetic Interference in High-Resolution Digital Audio Transmission Systems

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ABSTRACT

High-resolution digital audio systems are especially susceptible to sources of electromagnetic noise from the environment, for example, crosstalk from adjacent cables. The noise can induce errors and increase jitter in the recovered clock signal.

We discuss the most important noise sources and their characteristics. Next, we analyze the noise susceptibility of typical transmitter and receiver circuits. Test results are provided for a system with induced common-mode noise. The paper concludes with circuit design, component and application considerations.

1. INTRODUCTION

Progress in digital audio technology has increased resolution to 20…24 bits and sample rates to 96…192 kHz. Equivalent clock jitter has decreased to 10 - 100 ps. The system's sensitivity to noise and interference is increased proportionally. Interface designs which work fine in 16 bit consumer applications will not deliver the quality or interference rejection required in high-resolution professional applications in environments rich in noise sources. We discuss potential interference sources and how the interference couples into digital audio transmission systems. The interference affects recovered clock jitter, the data error rate and the conducted noise emission.

We analyze some typical interface circuits used in digital audio transmission systems. A new test method is presented for interference susceptibility

testing of these systems. The test fixture design and results are described in depth. Finally, we consider techniques to reduce the effects of interference. Carefully specified and applied transformers and passive filters are key to reducing noise and interference .

1.1. Digital Transmission Overview

Figure 1 is an unbalanced system with a transmitter (TX), cable and receiver (RX) such as described in AES-3id-2001 [1]. The cable shield reduces electrostatic interference. Since some common-mode noise voltage always exists between TX and RX ground returns, a common-mode current must flow through the shield along with the signal.

Figure 2 shows a balanced system including a shielded cable pair, such as described in AES3-1992 (r1997) [2, 3]. The TX output and RX inputs are differential. This is intended to provide rejection of common-mode noise coupled into the RX input.

The function of these systems is to transmit and recover data without errors, and to recover clocks with minimal increase in jitter. The author has discussed the use of transformers in digital audio systems in a previous paper [4] and developed a powerful measurement technique, Induced Jitter Histograms, for measuring the interference susceptibility of these systems [5].

Shielding and grounding technique has been discussed extensively in the literature [6, 7, 8,]. These papers are directed towards baseband audio, but the same basic principles apply to digital audio transmission systems. The high-resolution designer who seeks to approach theoretical performance should consider a system design using EMI noise reduction techniques, RF layout practice, grounding and shielding to achieve the best possible noise immunity and transmission fidelity.

1.1.1. Application to Separated Clocks

The AES/EBU and S/PDIF type formats embed clock and data in a single bit stream, and recover the clock with a phase-locked loop (PLL). Other transmission formats use separate clock and data (e.g. SDIF-2, “superclock”) to reduce recovered clock jitter by eliminating the PLL for clock recovery. The transmission system topology, measurement techniques and solutions discussed can be applied to either method of digital audio transmission.

2. INTERFERENCE GENERATION AND COUPLING

Digital audio systems are generally used in electrically noisy environments. Movie studios, broadcast studios and satellite uplinks are examples rich in interference sources. Stray capacitance and inductance provide coupling paths for the interference to enter the digital audio transmission path. Other entry points include radiated EMI, cross talk between signals and common-mode noise. Noise currents flow in either direction through any input or output.

2.1 Interference Sources

Digital clocks for DSPs and CPUs, video equipment, switching power supplies, wireless and wired computer networks are examples of conducted and radiated interference sources. The digital audio signal is intentionally limited in bandwidth, but out-of-band high frequency noise can nonetheless affect data transmission and clock recovery circuits. In large studios, the use of hundreds of signals on long cables (100-1000M) further increase the noise burden.

Switch-mode power supplies usually operate in the range between 20 kHz and 10 MHz. These supplies must meet regulatory requirements for radiated and conducted EMI, but they can emit sufficient interference to affect high-resolution systems.

Figure 3 is a two-channel, balanced system illustrating some of the noise sources and coupling mechanisms mentioned above. Figure 4 defines the normal (differential) mode and common-mode currents generated by an interference source [9]. Normal-mode current flows in a circuit from a source to a load and back, while common-mode currents are coupled equally into both conductors, and flow to the load via stray capacitances to ground.

2.2 Resistively Coupled Interference

Figure 5 illustrates resistive (or galvanic) coupling of noise between device #1 and #2 by common impedance shared in the return (“ground loop”). The common impedance depends on the length and copper area of the conductors such as PCB traces, ground planes, chassis to earth connections, etc.

2.3 Capacitively Coupled Interference

Figure 6 shows capacitive coupling between noise source #1 and device #2. The stray capacitance may represent adjacent cable pairs, PC board traces, etc. The degree of coupling depends on the stray capacitance and the load impedance at the receiver.

2.4 Inductively Coupled Interference

Figure 7 illustrates inductive coupling between two devices. Noise source #1 generates a current that drives load #1. Device #2 source drives input #2. Any circuit will have stray inductance proportional to the loop area encircled by the current flowing. A mutual inductance must exist between conductors #1 and #2 , increasing as the loop areas approach each other. This is in effect a transformer! Long cables with multiple conductors and circuits with large enclosed areas will have substantial coupling. Twisted pair cables reduce the loop area of the normal-mode current by changing the direction of the field with each twist. The mutual inductance between pairs is never zero, since the twisted wires must have some space between them (e.g. for insulation).

2.5 Common-Mode to Normal-mode Conversion

Balanced connections are intended to reject common-mode noise. Figure 8 shows a balanced system similar to Figure 4, with the addition of stray impedances to ground from either side of a balanced load. Common-mode noise current flows through the balanced cable, one-half of the total current in each conductor, if the stray impedances to ground were equal.

Since the stray impedances are never exactly equal, perfect balance cannot be achieved in practice. The common-mode current will produce a normal-mode noise voltage across the load, as shown by (1).

$$(1)\ V_{inDM} = \frac{Icm}{2} \frac{Z_{load}(Z_{1stray} - Z_{2stray})}{Z_{load} + Z_{1stray} + Z_{2stray}}$$

The normal-mode voltage depends on the degree of imbalance of the stray impedances to ground and the ratio of load impedance to the sum of the impedances to ground.

For example: Icm = 5 mA, Z_{load} = 5 kΩ, Z_{1stray} = 250 kΩ, and Z_{2stray} = 200 kΩ, V_{inDM} = 1.375 V.

In a typical receiver, the impedances to ground include bias resistors inside the IC and external to it, stray capacitances to ground and the junction capacitance of any protective diodes. Since diode junction capacitance is a function of applied voltage, there will be both dynamic and static unbalance of the impedances to ground. Other possible sources of unbalance can include capacitors, transformers, noise filters etc.

2.6 Unbalanced Inputs and Outputs

The unbalanced system in Figure 1 has no inherent rejection of common-mode noise. The common shield carries both signal and noise currents between the equipment chassis, which can cause noise and interference problems.

3. INTERFACE CIRCUITS

Confusion exists in the details of the interface circuit between the digital signal and the transmission cable. For example, industry standards [1-3] for transmission differ in the use and specifications of transformers. IC manufacturer's application notes and evaluation board circuits show wide variations in circuit design recommendations and parts.

It is very difficult to obtain the internal circuit details of digital audio ICs. The IC specifications reveal few details about the interface circuit. We reviewed several manufacturer's data sheets and discussed the circuits with the IC designers to clarify the topologies used. Balanced inputs and outputs are generally RS-485 compliant and single-ended interfaces are usually logic level requiring external drivers and receivers. We assume RS-485 type drivers and receivers are used in the ICs unless otherwise indicated on the spec sheets.

3.1. Analysis of Transmitter Circuits

Figure 9 shows the output stage of an RS-485 compatible driver similar to the SN75174 family. The half-bridge output stage is used in most digital audio transmitter ICs. The balanced outputs are complementary.

3.1.1. Sensitivity of TX to Induced Jitter

Conducted interference can enter the TX connection and contaminate signals used at other points in the equipment.

Figure 10 shows a balanced TX circuit with a transformer driving an AES/EBU output. Common-mode noise enters the cable by capacitive coupling.

The noise current flows through the transformer's primary-secondary capacitance C_S and into the TX IC outputs. A portion of this current will flow to either power or ground, depending on the instantaneous state of the IC output half-bridge.

The ground plane, power plane and IC connections have some inherent inductance and resistance. The common-mode noise current induces noise voltages on these parasitic impedances. This noise can affect clocks and data in other parts of the TX circuit.

3.2. Analysis of Receiver Circuits

Figure 11 shows a few RX IC manufacturer's suggested interface circuits. The upper two are balanced inputs, both with and without a transformer. The lower left is a typical S/PDIF single ended input. The lower right shows a more advanced balanced circuit, with a shielded transformer and overvoltage protection diodes.

RX ICs with single-ended inputs are CMOS compatible, and require external circuitry for all signal conditioning e.g. for common-mode rejection (CMRR). Figure 12 shows typical IC internal circuitry for balanced inputs. The most common circuit is a comparator with some hysteresis. The comparator has little capability for CMRR. The lower half of the figure has an input using two separate stages, typical of RS-485 ICs such as the SN75175 family. The A and B inputs are Schmitt triggers of opposite polarity, to provide a measure of noise immunity. There is no cross-coupling of the two inputs and hence no common-mode rejection.

3.2.1. Sensitivity of RX Input To Induced Jitter

Figure 13 shows a receiver with a common-mode noise source on the input. The noise current flows through the transformer primary-secondary capacitance C_S, to the IC inputs. The current is coupled to the RX IC power and ground through the impedances (in the IC or external) to ground and the stray capacitance from inputs to power and ground. This current generates noise voltages across the parasitic impedances between various points in the circuit and contaminates power and ground planes.

3.2.2. Noise Induced Jitter in Reclocking RX

Figure 14 has a reclocking stage to reduce the recovered clock jitter in the system of Figure 13. The flow of noise current through the power and ground planes contaminates the output of the reclocking stage, which increases the jitter of the clock output to the D/A converter.

3.3. The Effect of Transformers

The receiver interface requires a transformer to provide significant rejection of high frequency common-mode noise.

If a differential amplifier were used (e.g. external to the RX IC) its common-mode rejection (CMRR) will rolloff above the high frequency breakpoint. The CMRR of the transformer is inversely proportional to its P-S capacitance, so the high frequency rolloff of its CMRR is at a substantially higher frequency than that of the amplifier. Active circuitry cannot replace the transformer.

A low-capacitance transformer increases the impedance of the common-mode noise path. Optimized low-capacitance transformers can achieve 1 - 2 pF vs. 15 - 40 pF for ordinary types. Optimized transformers with interwinding (Faraday) shields can further reduce this capacitance to 0.5 - 1 pF!

Certain industry recommendations for transformer bandwidth are misleading. A well-designed transformer must have ample bandwidth and minimum pulse aberration [4]. Modern systems must operate over a wide range of Frame Sync (FS) e.g. 32 to 96 kHz or 192 kHz. The need to pass signal harmonics and maintain phase linearity requires a much wider bandwidth than is often assumed to be sufficient.

A previous paper [4] shows that the transformer's low frequency cutoff F_{low} affects jitter due to intersymbol interference. We recommend an $F_{low} = FS_{min}/3$, e.g. for 44 kHz FS_{min}, ~ 10 - 15 kHz. The high frequency cutoff F_{hi} should pass at least the 5th harmonic of the highest half-bit frequency, 128x FS_{max}. With a FS_{max} = 96 kHz, the half-bit rate is 12.288 MHz so the transformer F_{hi} should be at least 60 MHz. Optimally designed transformers have a bandwidth ratio F_{hi} / F_{low} of 3.5 to 4 decades, e.g. 10 kHz to 100 MHz.

Some designers attempt to use the transformer to limit the risetime of the signal. This approach is not optimal, due to tradeoffs in transformer design. A transformer with adequate bandwidth and low pulse aberration cannot also limit the risetime of the signal to the desired values. The overall risetime should be limited by other system components.

3.4. Simulation of Differential Amplifier

A computer simulation demonstrates the effect of transformer capacitance on RX CMRR. Figure 15 is a model of a transformer T1 driving a differential amplifier. A common-mode noise source is applied to

both sides of the transformer primary. This generates a noise current through the interwinding capacitance C1, which flows to both sides of the transformer secondary. The noise current through the amplifier input impedance R15/C2 results in a common-mode voltage at both (paralleled) inputs of the differential amplifier.

Figure 16 is a plot of the CMRR for this model. The parameter is the transformer interwinding capacitance C1. The upper trace is the CMRR of the amplifier alone (C1 = infinite). A high capacitance transformer (type X) with C1 = 25 pF, middle trace, provides some rejection at relatively low frequencies, 100 kHz – 500 kHz, but has little effect above 1 MHz.

The low capacitance shielded transformer (type S2) with C1 = 0.5 pF, lower trace, shows greatly improved CMRR throughout the frequency range. At 100 kHz transformer S2 shows an improvement of 34 dB in CMRR compared to the high capacitance transformer X. At frequencies above 10 MHz, transformer X provides 1 dB rejection, while the CMRR improvement of S2 is 16 dB compared to type X. The transformers mentioned here are shown in figures 36 and 37, and described below.

This result and plot shape are explained by the effect of the capacitive divider formed by the transformer self-capacitance and the input and stray capacitance of the amplifier.

4. INTERFERENCE EFFECTS

EMI, crosstalk and noise increase jitter and the recovered data's error rate. Other effects include power and ground plane noise contamination and reduced regulatory compliance for conducted emissions and circuit susceptibility. Transmit and receive circuits are both affected by common-mode noise.

4.1. Susceptibility of Interface Circuits

4.1.1. Sensitivity of Clocks To Induced Jitter

Sampling clocks determine the instant of A/D or D/A converter sample time. Jitter in the sample clock must result in a corresponding error in the digitized or reconstructed audio. Equation (2) is a calculation based on dv/dt for a system of N bit resolution and an audio signal sinewave of radian frequency ω. The sampling time error, t_e is inversely proportional to signal frequency and resolution [10 - 15].

$$(2)\quad t_e = 2^{1-N} / \omega$$

The example in (3) calculates the time error for a full scale 15 kHz sinewave digitized to 20-bit resolution. The LSB equivalent sample time error is 20 ps!

$$(3)\quad t_e = 2^{-19} / 30k\pi = 20.24\,ps$$

4.1.2. Decoded Data Errors

Figure 17, upper trace is the eye pattern at the input of an RX IC with a differential probe from RXP to RXN, taken without any common-mode noise.

In the lower trace of Figure 17, common-mode noise is applied to the inputs via the cable and coupled through a high capacitance transformer X. The noise closes the eye pattern considerably and increases the RX clock jitter.

4.2. Common-Mode Rejection (CMRR) of Interface Circuits

Single-ended RX inputs have no common-mode noise rejection. Most balanced receiver circuits use Schmitt triggers to provide a measure of noise immunity, but have little or no common-mode noise rejection; transformers must be used to provide this function. Transmitter ICs are also susceptible to common-mode noise and require transformer isolation to reject such noise.

4.3. Power Supply and Ground Plane Noise Contamination

Both TX and RX sides of a system serve as paths for common-mode noise currents passing into the IC input/output pins. The currents flow through the IC and into power and ground planes contaminating other circuitry.

This problem is more severe on the TX side since the output is connected to either Vcc or ground, depending on the state of the transmitter input. The noise is modulated by the signal applied to the TX IC half-bridge transistors.

4.4. Regulatory Compliance

All electronic equipment requires regulatory compliance for conducted and radiated interference emission [16]. Some regulations provide for testing of the conducted interference susceptibility of equipment to such noise.

4.4.1. Circuit Susceptibility

IEC 61000-4-6 [17] is a conducted immunity standard, tested with interference intentionally applied to the equipment's input and output cables, while the interference frequency is swept over a wide range. The equipment should operate properly despite the applied interference.

4.4.2. Conducted Interference Emission

Many national and international regulations cover the emission of EMI for various types of equipment. Compliance with conducted emission requires noise levels on all connectors and cables to be limited according to frequency and equipment type [16, 17].

The same basic principles governing noise susceptibility apply to EMI emission. For example, a balanced cable with transformer-coupled output will also isolate common-mode noise emitted from the equipment [18].

5. MEASUREMENT TECHNIQUES

Equipment manufacturers and designers often neglect to test for interference susceptibility. It is difficult to characterize a complete digital audio system for noise susceptibility because of the effects of encoders, decoders, clock recovery phase lock loops, etc.

We approached the problem of interface testing by simplifying the digital audio system to just the transmission TX and RX ICs interface and the transmission cable. We use a squarewave at the half-bit rate 128x FS instead of the AES/EBU signal.

A balanced output is generated with an RS-485 TX IC. This output is coupled to a multi-paired balanced cable and then to an RS-485 receiver. Common-mode noise is injected into the cable and the effects observed.

A network analyzer, statistical counter, digital scope and time interval analyzer connected to the output characterize the effects of noise and interference on the test fixture's transmission system. The induced jitter histogram technique employed was described by the author in a previous paper [5].

5.1. CM Interference Test Fixture

Figure 18 shows the details of the test fixture. A low jitter squarewave at 128x FS drives the RS-485 TX. The complementary outputs are AC coupled to a balanced attenuator to match a 110 Ω impedance. A 1:1 transformer connects to a 31-m length of CAT 5 cable. The transformer is mounted on an IC header, and is easily changed by using a ZIF socket.

The cable has 5 pairs, one for the signal and 4 other pairs paralleled together to a common-mode interference source, applied through a wideband isolation transformer to break ground loops. The noise source may be connected to either the TX or RX end of the cable.

The output of the cable pair carrying the signal is transformer coupled, with that transformer also mounted on a ZIF socket. The transformer secondary is terminated with 110 Ω and applied to the input of the RS-485 RX. The output of the RX IC is connected to the counters, time analyzer and scope.

Both TX and RX terminations are center-tapped to allow observation of the common-mode noise at that point. The RS-485 ICs include 10 Ω current sampling resistors in series with their power and ground pins. A probe samples the voltage across the 10 Ω resistors to observe noise currents to power and ground. The probe connects to the network analyzer's input via AC coupling capacitors and a 39 Ω matching resistor through a 50 Ω cable. The AC coupling allows checking of the +5V supply noise current.

5.2. Application of Network Analyzers

An Agilent HP3577 Network Analyzer is used to test the effect of common-mode noise over a wide frequency range. The analyzer source drives the common-mode input of the test fixture, and the 4 unused cable pairs. The source is leveled using an HP35676A divider (a precision splitter/directional coupler) to sample the source voltage and to drive the analyzer's reference input.

The impedance mismatch represented by the cable's capacitance (resonance as well as standing wave effects) causes the analyzer's source to fluctuate widely as the frequency is swept. This mismatch is compensated for by normalizing the analyzer to a circuit omitting the transformer. A shorting plug replaces the transformer and the network analyzer is swept through the desired frequency range, e.g. 100 kHz to 100 MHz. The measurement with the shorting plug is normalized to 0 dB, the upper line of the

reference grid. The transformer is then replaced and the analyzer swept again. The result is a direct plot of the common-mode noise rejection increase due to the transformer.

One test with the analyzer is rejection of common-mode noise in power and grounds. The CM noise current enters both TX and RX circuitry through the cable and the self-capacitance of the transformers on both sides of the cable.

The analyzer is connected via the probe to TX or RX IC's power or ground current sampling resistor. The input signal to the TX IC is either grounded or held high to remove the modulation effect of the transmitted signal from the noise. The TX output stage passes the noise current to either the ground or power plane.

5.3. Jitter Measurement Equipment

Figure 19 shows specifications of various types of equipment for measuring jitter. Since the peak-to-peak, weighted jitter [12, 14] cannot be tested by most of this equipment, we elected to measure the RMS wideband jitter, which is the standard deviation σ, of a sample set of periods. The results are fine for comparisons and can be correlated to the weighted P-P jitter.

The simplest technique uses a time interval counter with statistics setup to measure the period, and to take a set of samples (e.g. 500 - 5,000). The HP5370B counter (circa 1970s!) has 20-ps residual jitter. Later versions, e.g. HP5372B and Stanford Research Systems SR620, can display time variation of the period and also jitter histograms. The HP5372B has a CRT display while the SR620 uses a numeric display and outputs graphics to an external scope. Residual jitter and resolution of these instruments is ~100 ps.

Time interval analyzers have been specifically developed for telecom and CD/disk drive measurements. These instruments provide convenient statistical analysis and dedicated jitter histograms. A good example is the Yokogawa TA320/520/720 series. The TA320 was employed in these tests.

A wide range of digital oscilloscopes (DSO) are available, some of which are capable of jitter measurements. In most, memory, software or firmware options are required to provide these functions. Tektronix TDS5000 and TDS7000 series and LeCroy Wave Runner/Wavepro are examples.

In DSOs, the residual jitter and histogram resolution depends on signal frequency, memory depth and other characteristics of the particular scope selected. Signals at frame sync frequencies can typically be analyzed with 10 ps to 100 ps resolution. Due to trigger jitter, memory depth and software, these scopes can be rather costly and complex to setup compared to the counters and dedicated analyzers discussed.

5.4. Induced Jitter Histogram Technique

This technique was developed by the author to provide a sensitive test of the effect of system components such as transformers on common-mode noise rejection [5]. Interference is applied to a transmission system similar to the test fixture described above. The interference source couples common-mode noise into the RX via the transmission cable.

The receiver output goes to the time interval analyzer to measure the jitter and the shape of the period histogram. The histograms in figures 23 - 32 show the mean period at the center of the horizontal axis and the deviation from the mean in increments of 100 ps per bin. The vertical axis is the number of samples in that bin. The Jitter Histogram is effectively a probability distribution of a sample set of periods centered around the mean period. This is a very sensitive test for comparison of the common-mode noise rejection of transformers, cables, receivers, differential amplifiers and other devices in the signal path.

6. MEASUREMENT RESULTS

The test fixture was operated with a 6.144 MHz test signal and either a 3.6 MHz interference source or the network analyzer, swept up to 100 MHz. Various transformers were used in both TX and RX. Observations at one side of the system were made with the best low-capacitance transformer on the opposite side. Data taken includes scope photos at several points, network analyzer plots of power and ground noise current vs. frequency and jitter histograms taken at both transmit and receive locations.

6.1. Test Fixture Waveforms

Figure 20 shows the input to the transmitter IC and the common-mode noise observed at the primary of the TX transformer. This demonstrates the effect of common-mode noise coupled into the cable.

Figure 21 shows the noise seen at the RX IC input. The high capacitance transformer X passes substantial noise, while low capacitance transformer S2 attenuates most of the noise.

6.2. Network Analysis Plots

Figure 22 is a plot of common-mode noise current to ground at the RS-485 TX IC, referred to a circuit without a transformer. The sharp peaks and dips are due to resonance (e.g. transformer inductance and cable capacitance) and mismatch of the common-mode impedance to the network analyzer output impedance. The test was normalized to the upper grid reference line. The reference level at 3.544 MHz, (no transformer) was 614 uA RMS of noise current at the TX IC return pin. The rolloff below 100 kHz was due to the very low signal levels at these frequencies.

Transformer X provides 8 dB of attenuation at low frequencies and virtually none at high frequencies. Shielded low-capacitance transformer S2 increases common-mode rejection to over 20 dB at frequencies up to 15 MHz and still provides 10-20 dB of improvement up to 40 MHz. Similar results are seen at the power pins of the ICs. The rolloff of both curves above 50 MHz may be an artifact of the test, to be investigated in the future.

6.3. RX Induced Jitter Histograms

RX tests were performed using low-capacitance transformer S1 on the TX side. The system residual jitter is 150 ps, representing the noise in the RS-485 ICs, the signal generator and the internal noise of the analyzer. The effect of transformers on the RX side was observed by changing the RX transformer. The output of the RX IC is analyzed by the Yokogawa TA320 time interval analyzer.

Figure 23 shows the induced jitter without any transformer. Common-mode noise induces a jitter of 1.505 ns RMS. Figure 24 shows the results with a high capacitance transformer X at the RX. The jitter is 3.104 ns and the histogram is uniformly distributed with peaks at the extreme ends.

Figure 25 shows the RX output jitter using a high capacitance shielded transformer Y at the RX. Jitter has increased to 7.83 ns. The histogram shape indicates a sine variation of period with time. The phase response of this transformer may account for the result. Figure 26 is the result using optimized low-capacitance transformer S1, with 297 ps jitter and a nearly ideal Gaussian histogram.

6.4. TX Induced Jitter Histograms

The effect of common-mode noise on the TX side was observed by placing the time analyzer at the primary side of the TX transformer. Common-mode noise on the cable induces jitter at that point by passing current through the transformer self capacitance. Several types were used for the TX transformer, while keeping low-capacitance transformer S1 on the RX input.

Figure 27 was taken with no transformer and shows jitter of 19.367 ns with a scattered histogram of many discrete periods. Figure 28 uses a high capacitance transformer X with 85 ns of scattered jitter. Figure 29 shows low capacitance unshielded transformer S1, which reduced the jitter to 1.64 ns. Figure 30 used a very low-capacitance shielded transformer S2, with jitter 302 ps and a nearly ideal Gaussian histogram.

6.5. Interpretation of Jitter Histograms

The shape of the jitter histogram reveals the nature of the variation of clock period about the mean value. Figure 31 shows several patterns:

Upper: Gaussian distribution of period is random.
Middle: Bi-value Gaussian, periods distributed normally about two discrete periods.
Lower: Sinewave variation of period with time.

Figure 32 has more examples:

Upper: Very Narrow Gaussian (residual jitter)
Second: Symmetric Period Variation
Third: Uniform Period distribution
Lower: Multiple Discrete Periods

7. RECOMMENDATIONS FOR IMPROVEMENT

7.1. Applications of Transformers

These results prove the transformer's dramatic effect on system performance when noise is present. Both TX and RX sides should use low-capacitance or shielded low capacitance transformers. The bandwidth of the transformer must be adequate for the maximum sample rate anticipated, e.g. for 192 kHz sample rate, the bandwidth should be at least 125 MHz. Low pulse aberration requires control of the transformer's phase linearity. If a shielded transformer is used, the shield should be tied to the ground plane, near the connection to the IC return pin.

7.1.1. Interstage Transformer Applications

Figure 33 is a modification of Figure 14 with a transformer added between the reclocking stage and the DAC to break the path of common-mode noise current. This technique reduces contamination of the reclocking stage's output clocks. The same technique can be used to couple clocks or signals from a transmit side IC to other stages. This avoids contamination of the clocks and data by common-mode noise coupled from the output connector.

7.1.2. Balanced System Using Shielded Transformers

Figure 34 is the balanced system of Figure 2 with the addition of shielded transformers on both transmit and receive sides. 30 - 40 dB of improvement in CMRR and noise immunity can be obtained at both sides of the system.

7.1.3. Unbalanced System with Transformers

Unbalanced systems use the cable shield as the signal's return path. They have substantial noise susceptibility due to noise voltage between the transmit and receive equipment grounds. The situation is improved by inserting transformers. Figure 35 is the unbalanced system as in Figure 1, with 2:1 ratio transformers on both TX and RX sides to improve noise rejection and provide 6 dB of step-up of received signal level [4, Fig. 18].

The transformers provide a balanced connection to the TX and RX ICs. This breaks the path for common-mode noise current in the cable shield. The circuit allows use of unbalanced coaxial cables and connectors, while providing the benefits of the reduction of common-mode noise by the transformers.

7.1.4. Comparison of Digital Audio Transformer Parameters

Figure 36 compares the parameters and performance of a wide range of commercially available digital audio transformers. The 4 parts tested with jitter histograms in the figures are identified by the *. Those include: high capacitance model X, low cost, shielded type Y, optimized very low-capacitance part S1 and optimized, shielded low-capacitance transformer S2.

The capacitance of the shielded transformers was measured with a guarded high frequency bridge: it is the effective capacitance from primary to secondary with the shield grounded. Common-mode rejection was checked at 6 MHz using the network analyzer. Pulse aberration was measured with a low aberration generator and digital oscilloscope in a precision constant impedance test fixture connected to the scope via a precision 50 Ω cable.

The design and construction of a transformer has substantial effects on its performance. Figure 37 illustrates some typical transformer internal details and construction. The winding design, and material quality and assembly technique determine the capacitance, leakage inductance and pulse aberration.

Plastic injection molded parts such as model X (Figure 37A) usually contain small toroidal cores (Figure 37B) with primary and secondary very closely spaced, resulting in high self-capacitance. The plastic molding has a dielectric constant (K) of 3.2 to 4.5, which increases the interwinding capacitance. Common-mode rejection and pulse aberration suffer greatly.

E core transformers generally have lower self-capacitance and better performance than toroids, but great differences exist in these types. Most are random wound by automated machine and varnish impregnated such as Part Y (Figure 37C). The varnish dip increases the self-capacitance. The result is usually better than the toroids, but still far from optimal. Model Y has a relatively low shielded capacitance, but performs rather poorly as indicated in the chart of Figure 36 by its high jitter, pulse aberration, and ratio error.

The best transformers for digital audio transmission use very high quality core and bobbin materials and precision optimized windings to yield superior results. Transformers S1 and S2 (D) are examples which are optimized for very low capacitance and excellent pulse aberration. They have the lowest possible self-capacitance compared to the other types. The trade off is cost vs. performance [4, 5].

7.2. Transient Protection

Digital audio transmitter and receiver ICs generally do not have much transient protection. The inputs and outputs may be clamped to power and ground with internal protective diode junctions, but excess currents or voltages can easily damage those junctions. RS-485 interface ICs have a higher level of protection, including internal protective Zener junctions to limit the transient voltage, but are not "bulletproof".

The use of transformer isolation provides the highest level of common-mode transient protection due to the low capacitance, high CMRR and the barrier provided by the insulation between windings (500 - 1500 V). Note that digital audio transformers are not designed or rated for safety (power mains) barrier application!

7.3. Filter Considerations: Common-Mode Chokes and Beads

Interference susceptibility at high frequencies can be improved by the use of ferrite beads and common-mode chokes. Figure 38 shows an improved receiver circuit with shield beads, a common-mode choke and a shielded transformer.

7.2.1 Common-Mode Chokes

At frequencies above 20 MHz, the interference suppression of even the best transformer will begin to roll off, since it is impractical to reduce primary to secondary capacitance much below ~ 1 pF. An improvement is to add a small common-mode choke between the connector and the transformer, as shown in Figure 38. These chokes must be selected to provide the desired attenuation at frequencies where the transformer common-mode rejection begins to fall off, but must not affect the desired signal's amplitude or phase characteristics. Ferrite cores can be wound to make this part, or ready-made CM chokes can be used.

The common-mode choke consists of a ferrite bead or small toroid, composed of wide band RF ferrite material. The balanced signal conductors are wound through the bead or toroid using a twisted pair wire (bifilar). Several turns are used to increase the inductance. The normal-mode signal travels up one wire and back through the other, canceling the magnetic flux in the ferrite core, so there is no effect on the normal mode signal. Common-mode noise current flows in the same direction through both wires and encounters the high impedance of the choke inductance. 30 - 1000 Ω are typical common-mode choke impedances. Figure 39, upper half, shows the dimensions and impedance of a bead core with 1 turn and a finished common-mode choke made using that core.

The lower half of Figure 39 shows a commercially available SMD CM choke. Manufacturers such as TDK and Murata make both through-hole and SMD chokes. CM chokes also have some DM mode inductance, and certain models are specifically designed to combine both functions in a single device by maximizing the differential inductance. "Data Line" filters are available which include CM/DM chokes and capacitors combined in one package to reduce parts count and PCB footprint.

7.2.2 Ferrite Shield Beads and Capacitors

Separate ferrite beads on each signal conductor can be used to protect against differential-mode interference above the desired signal passband.

The small capacitors placed after the chokes (both differential and common-mode) create two-pole L-C filters to increase the rolloff from 6 to 12 dB/octave above the cutoff frequency. The combination of normal-mode and common-mode chokes plus the common-mode rejection of the shielded transformer provides the maximum attenuation of interference. Extensive literature on EMI filter design can be consulted to optimize these filter components [19].

7.2.3 Reciprocity

The noise rejection provided by the transformer, bead, common-mode choke, etc. affects the noise current flow regardless of the location of the noise source. Due to reciprocity, the suppression measures taken to protect against external EMI and incoming CM noise will also attenuate internally generated interference, and reduce the conducted noise emission leaving the equipment over the digital audio cables. These techniques can be applied at both transmitter and receiver. Note that the degree of attenuation will be different for each direction, due to the different source and termination impedances as seen by the filter.

7.4. PCB layout

Figure 40 is a suggested PC board layout technique to achieve maximum isolation between primary and secondary of the transformer. The ground plane is split under the transformer and the secondary of the transformer goes to the RX IC input via short traces. The shield of the transformer is connected to the

ground plane half at the secondary side of the transformer. One layout technique is to use a "star" connection of several ground planes, to minimize the effect of noise currents in the ground planes.

7.5. Receiver Termination

Receiver circuits are normally terminated at the IC input pins after the transformer and/or passive filters (combined into a passive network for this discussion). The secondary termination damps the inductances and capacitances of the network, thus reducing pulse response ringing and smoothing the frequency response. The input impedance at the connector will be affected by the passive network, causing the impedance to deviate over the frequency band from the ideal resistive value. With secondary termination we have a tradeoff between CMRR and the effect on impedance.

Moving the termination to the input connector gives a nearly ideal resistive load, but the passive network will be undamped and "ring", the amount of pulse aberration depending on the filter components.

We have developed a solution using double termination. A portion of the termination resistance is placed on either side of the passive network, with the parallel combination equal to the desired termination impedance. In fig 41, a 110 Ω input impedance is realized with 165 Ω input termination Rin and 330 Ω at the IC input, Rsec.

Rin swamps the reactive effects of the network and Rsec damps the ringing. Figure 42 illustrates the improvement (plotted as the reflection coefficient) over a 10 kHz to 100 MHz band. The usual secondary termination of 110 Ω is the upper trace while the double termination is the lower trace.

8. CONCLUSIONS

The circuitry of a high-resolution digital audio interface is especially sensitive to common-mode noise, crosstalk and electromagnetic interference. The design of interface circuits and printed circuit board layouts must consider this interference susceptibility to realize high quality, low jitter transmission of digital audio signals.

New product designs should be tested for interference susceptibility to detect and debug the effects of noise and interference on clock jitter and data errors.

Commonly used transmitter and receiver ICs have limited (if any) ability to reject the common-mode noise. One effect of the noise is increased clock jitter.

The noise rejection of single ended ICs can be improved by the use of RS-485 transmitters and receivers and balanced connections with transformer coupling. Clock outputs from reclocking stages are also susceptible to contamination by common-mode noise and EMI interference through their power and ground connections.

High-resolution systems should use high-quality, low-capacitance, low-aberration transformers at both TX and RX sides. The noise rejection of a transformer is a function of its interwinding capacitance, interwinding shields and the receiver common-mode impedance. Use of an optimized transformer will improve common-mode noise rejection, reduce jitter and reduce noise contamination. Another benefit is greatly increased immunity to common-mode voltage transients.

Passive filter components such as beads, common-mode chokes and shunt capacitors can further improve the noise immunity and CMRR of a design.

ACKNOWLEDGMENTS

The author wishes to thank Dr. Richard Redl of ELFI S.A., Dr. Markus Erne of Scopein Research S.A., Dr. Steven Harris, and James A. Moorer for their very kind assistance, comments and support.

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Fig. 1 Unbalanced Transmission System

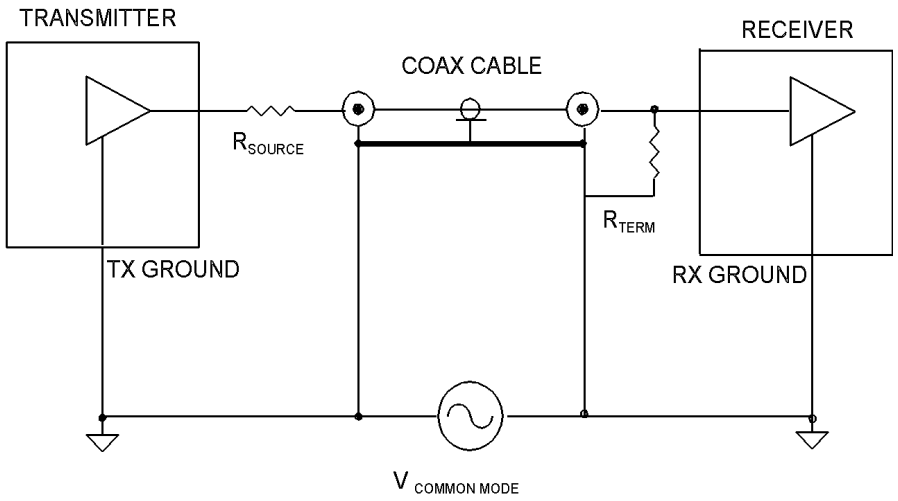


Fig. 2 Balanced Transmission System

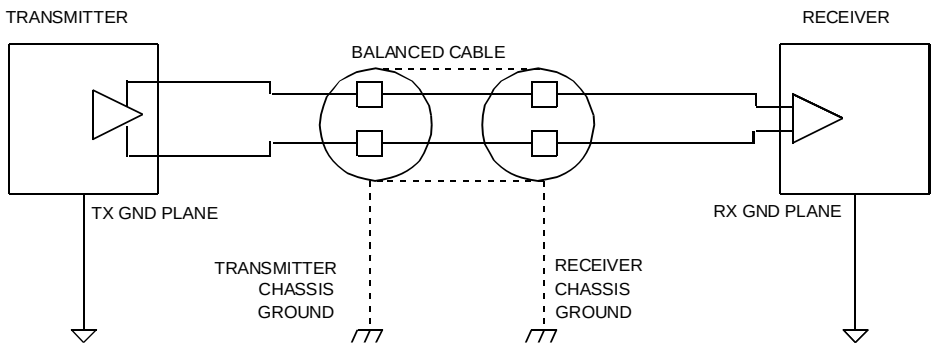


Fig. 3 Balanced Transmission System with Noise Sources

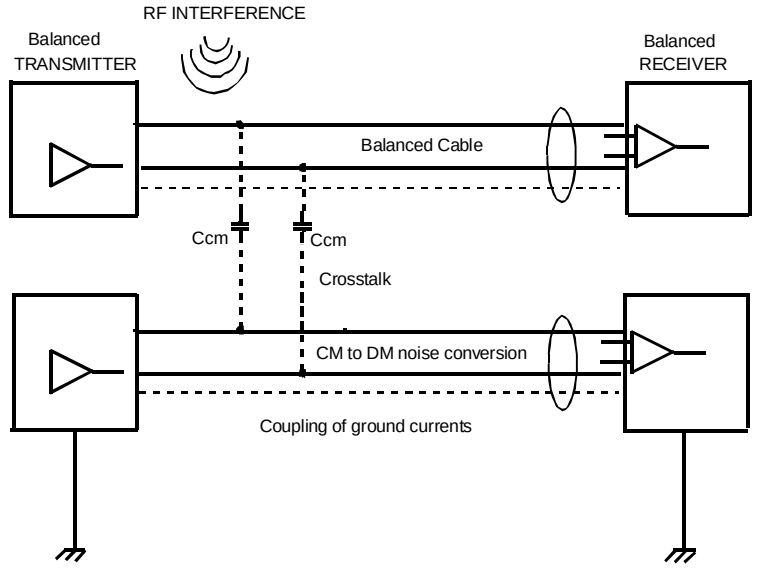


Fig. 4 Normal-Mode and Common-Mode Currents

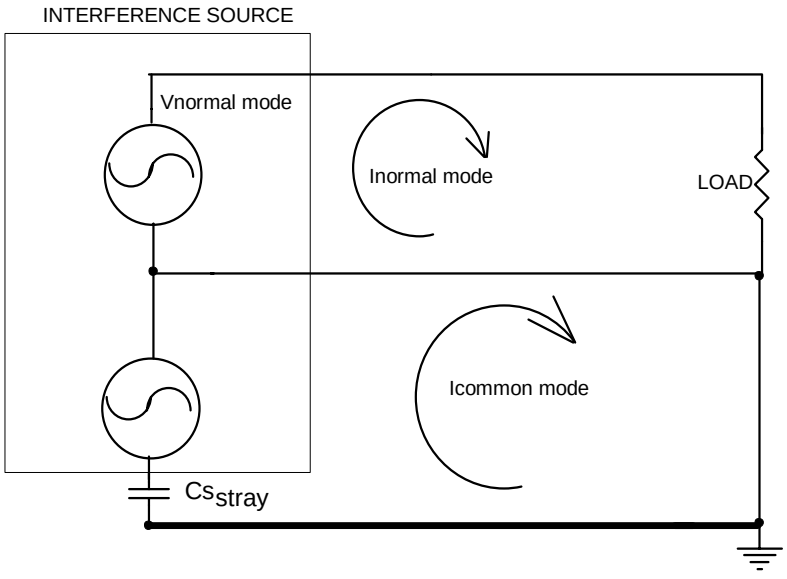


Fig. 5 Resistive Coupled Interference ("ground loop")

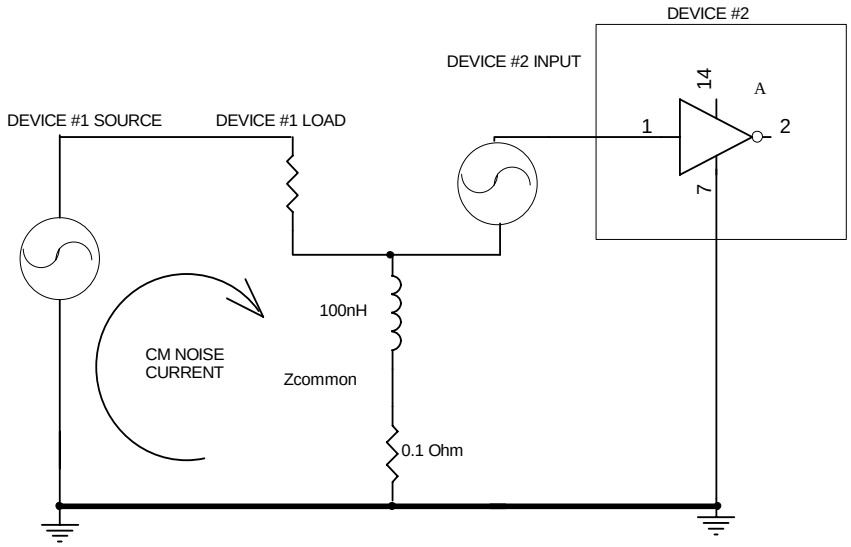


Fig. 6 Capacitive (Electric) Coupled Interference

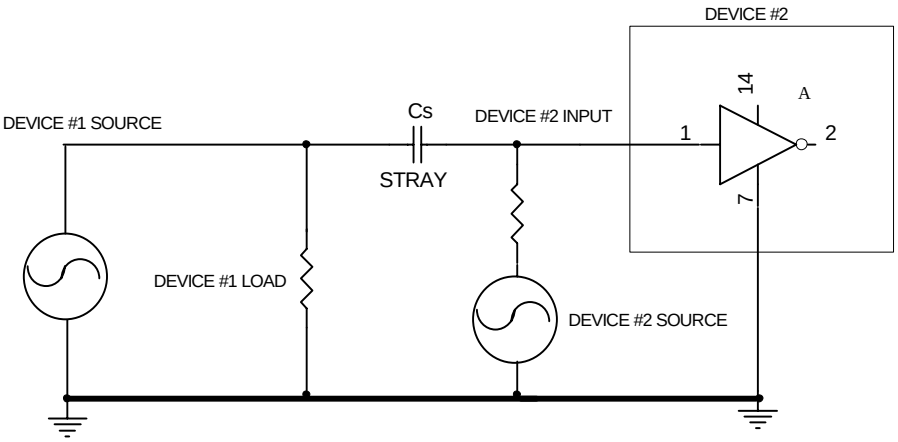


Fig. 7 Inductive (magnetic) Coupled Interference

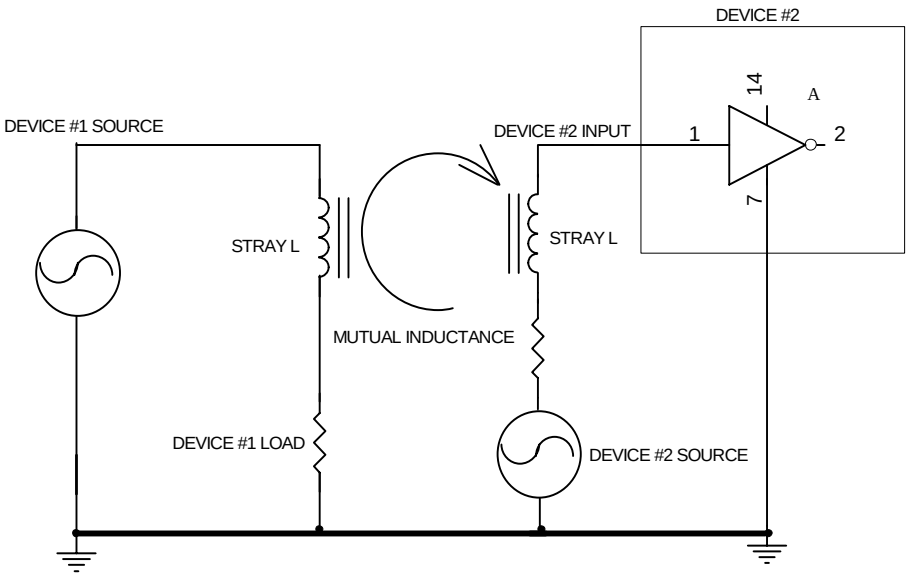


Fig. 8 Common-Mode to Differential-Mode Conversion

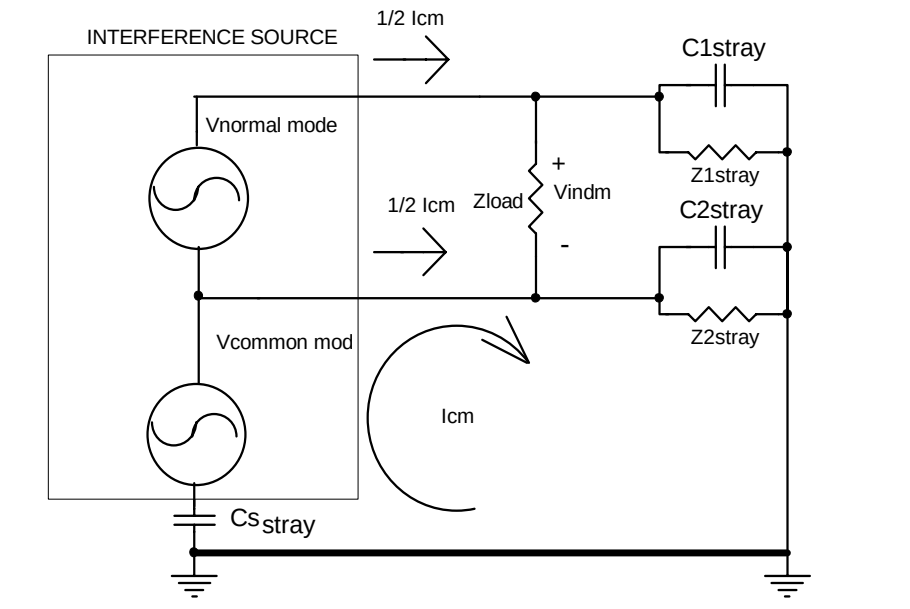
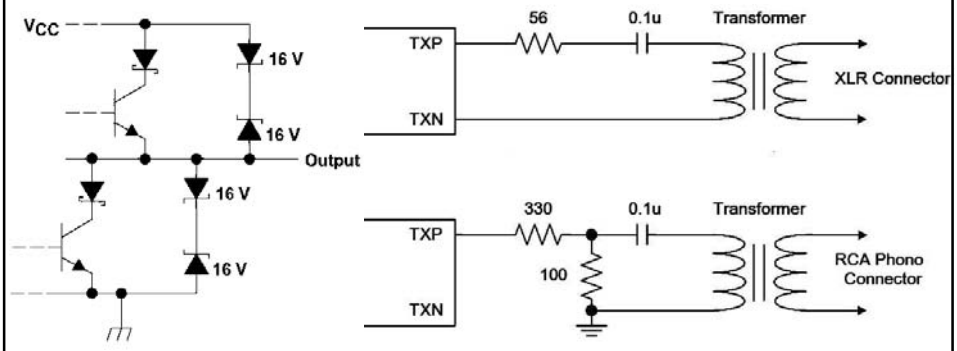


Fig. 9 RS-485 Output Driver and IC Manufacturer's Suggested Circuits



RS-485 Output Driver AES/EBU and S/PDIF Output Circuits

Fig. 10 Transmitter Common-Mode Noise/EMI Current Paths

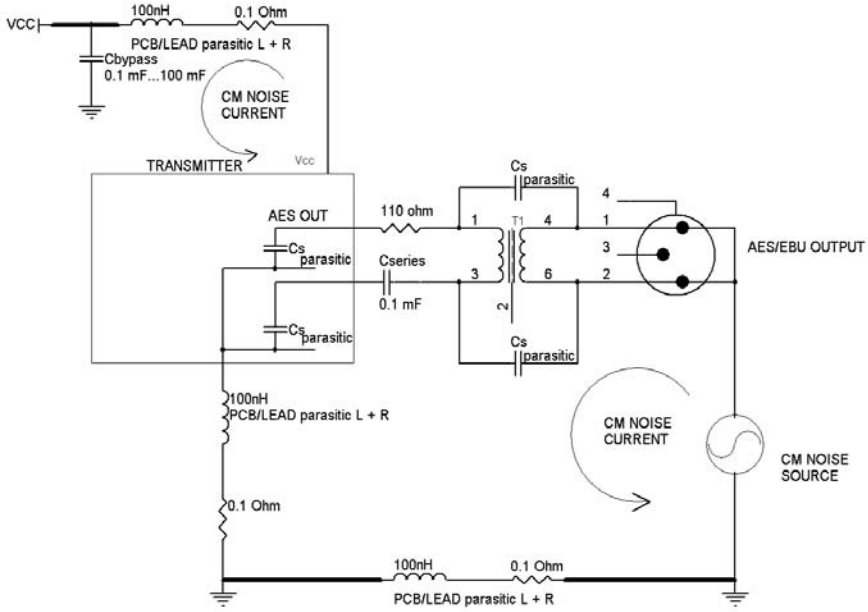
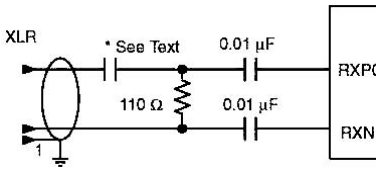
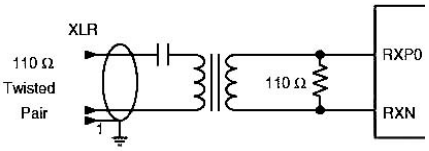


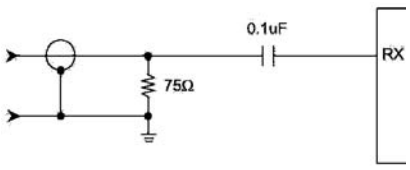
Fig. 11 RX IC Manufacturer's Suggested Circuits



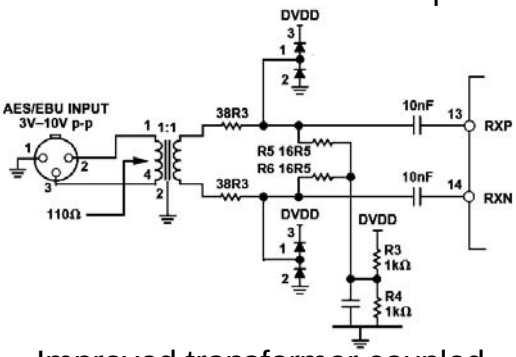
AES/EBU "Transformerless"



Minimal Transformer Coupled

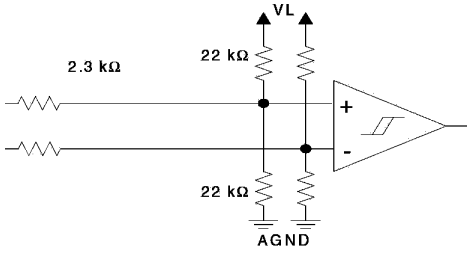


S/PDIF unbalanced 75 Ω

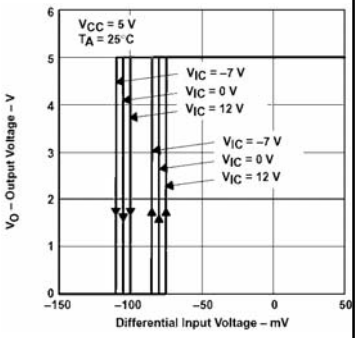


Improved transformer coupled

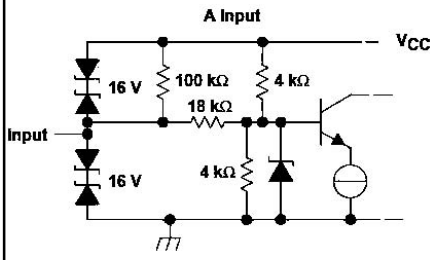
Fig. 12 RX and RS-485 Input Circuit, Transfer Function

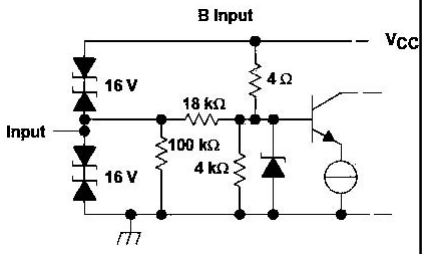


AES/EBU IC RX Input



RS-485 Transfer Function





RS-485 Input Circuit

Fig. 13 Balanced RX Common-Mode Noise Current

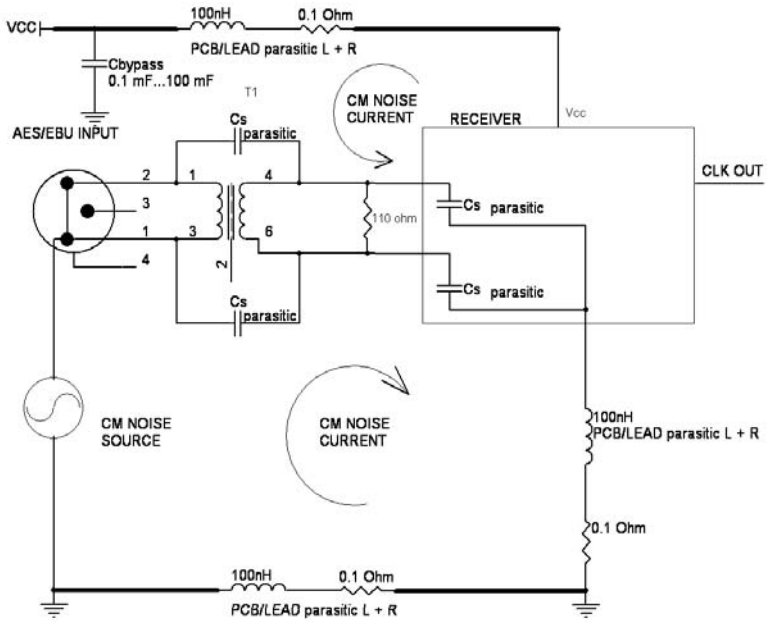


Fig. 14 Receiver with Reclocking Stage Common-Mode Noise Current Paths

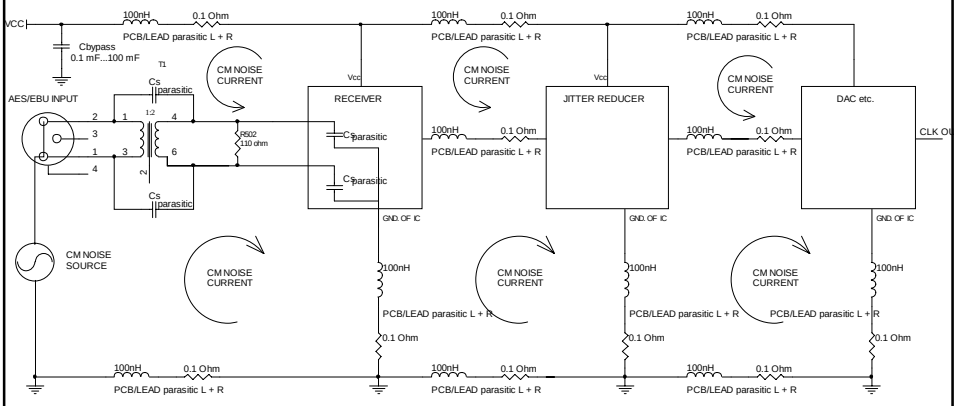


Fig. 15 Simulation Model of Common-mode Gain of Transformer + CMOS Differential Amp.

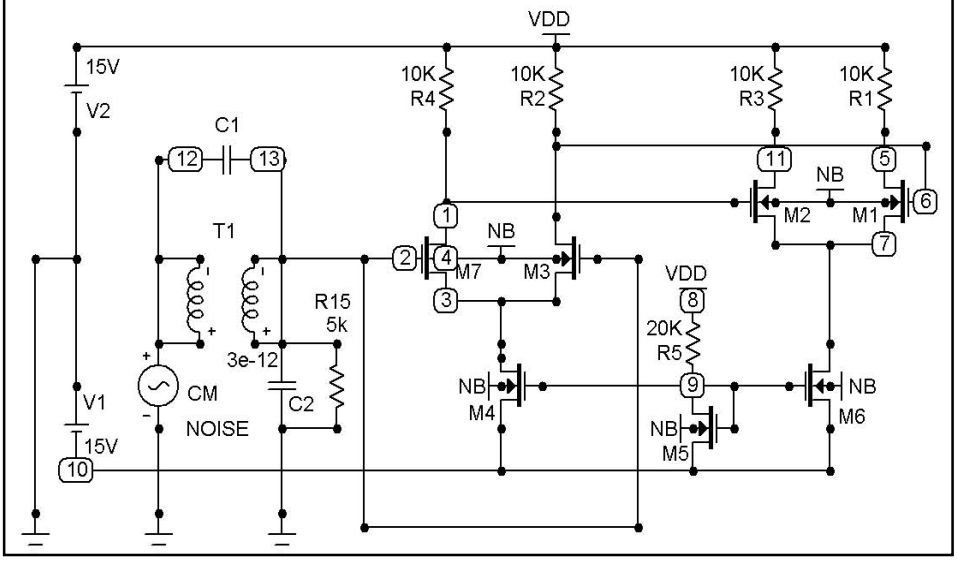


Fig. 16 Transformer and Differential Amplifier Simulation of CMRR vs. Frequency

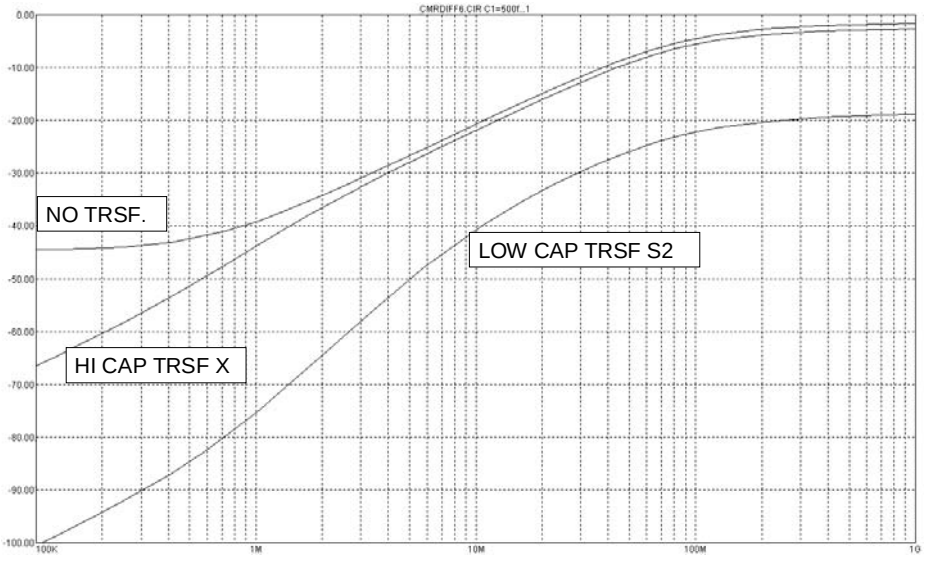


Fig 17. RX Differential Signal Eye Pattern with Common-mode Noise

NO CM NOISE

3.6 MHz CM NOISE

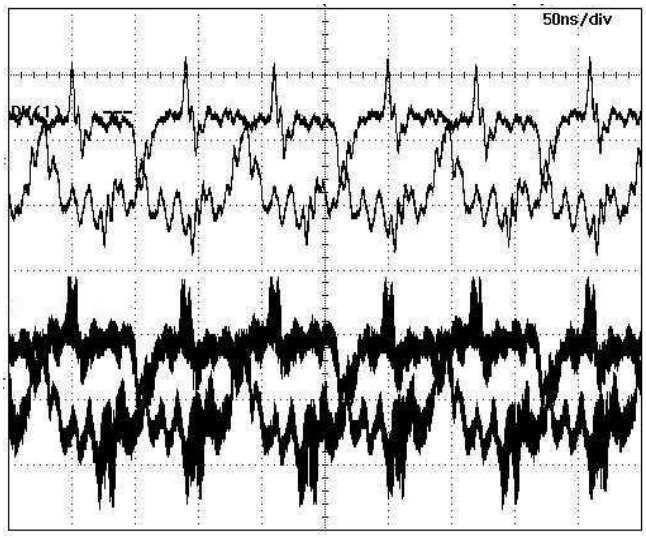


Fig. 18 Common-mode Interference Test Fixture

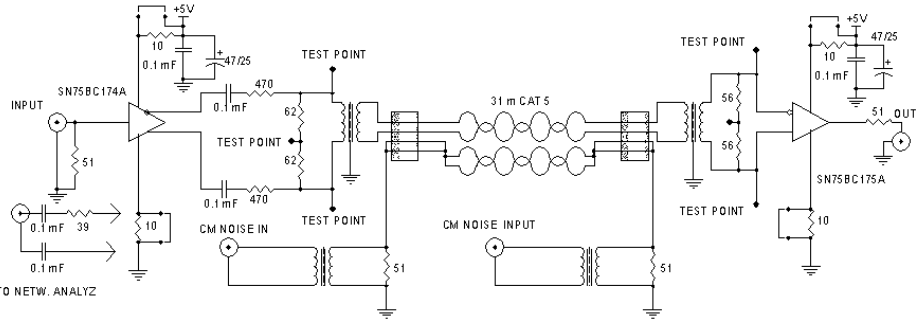


Fig. 19 RMS Jitter and Histogram Test Equipment

Type	Time Interval Counter	Time Interval Counter	Freq/Time Interval Analyzer	Time Interval Analyzer	Time Interval Analyzer	Time Interval Analyzer	DSO	DSO
Manufacturer	SRS	Hewlett Packard	Hewlett Packard	Yokogawa	Yokogawa	Yokogawa	LeCroy	TDS
Model	SR620	5370B	5372B	TA320	TA720	TA520	Waverun LT262 JTA	TDS5032 TDS7154
URL	srsys.com	testequity.com	testequity.com	yokogawa.com	yokogawa.com	yokogawa.com	Lecroy.com	tek.com
Output Formats	LED numeric, ext histo	LED numeric	CRT, histo, time plot	LCD, histo, time plot	LCD, histo, time plot	LCD, histo, time plot	LCD histo, time plot	LCD histo, time plot
Max Frequency	300 MHz	100 MHz	500 MHz	14 MHz	80 MHz	43 MHz	350 MHz	To 1 GHz
RMS Jitter	25 ps	20 ps	100 ps	100 ps	100 ps	100 ps	100 ps	To 10 ps
Resolution	100 ps	20 ps	100 ps	100 ps	25 ps	25 ps	100 ps	100 - 200 ps
Relative Cost	$4000	$500-4,000	$900-5,000	$10,000	$28,000	$19,000	$7,300	$11,000, $28,500

Fig. 20 Common Mode Noise at TX

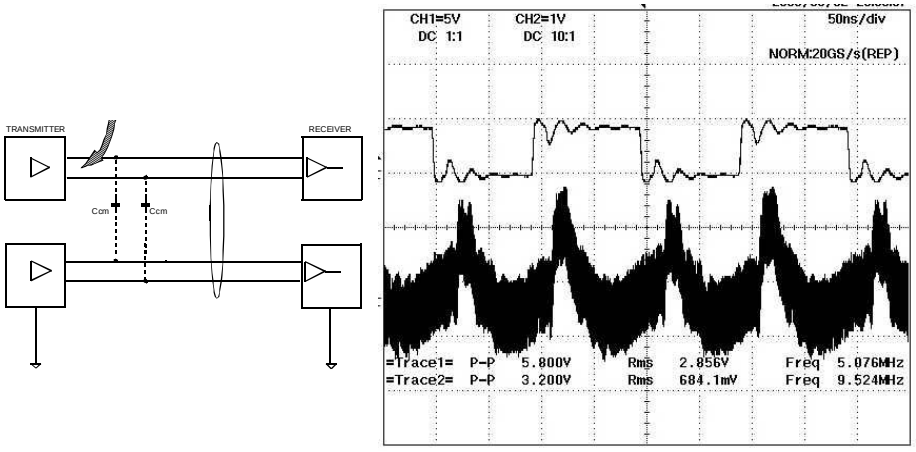


Fig. 21 RX Inputs With CM Interference

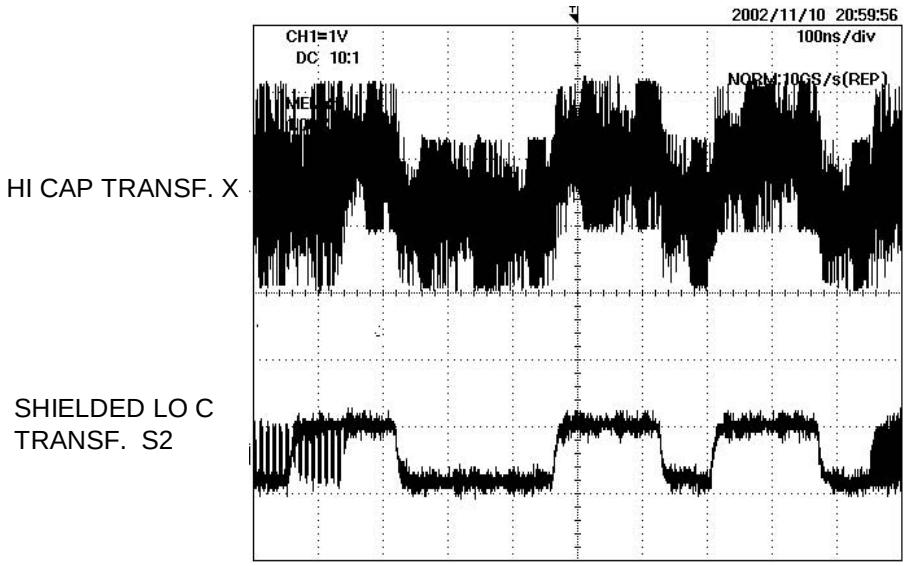
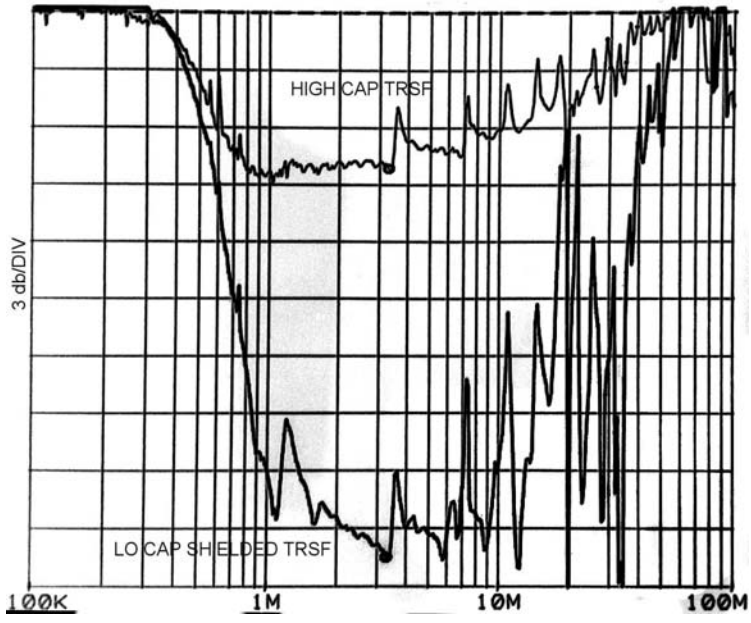


Fig. 22 TX IC Power CM current
Hi Cap Trsf X vs. Shielded Low Cap Trsf S2



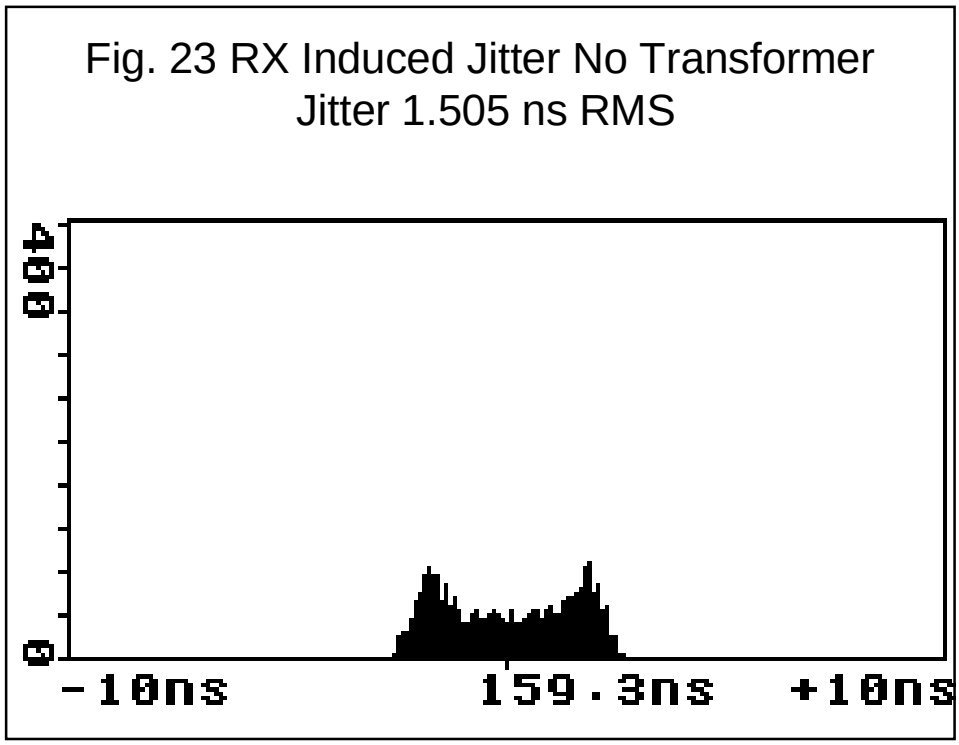


Fig. 23 RX Induced Jitter No Transformer
Jitter 1.505 ns RMS
-10ns
159.3ns
+10ns

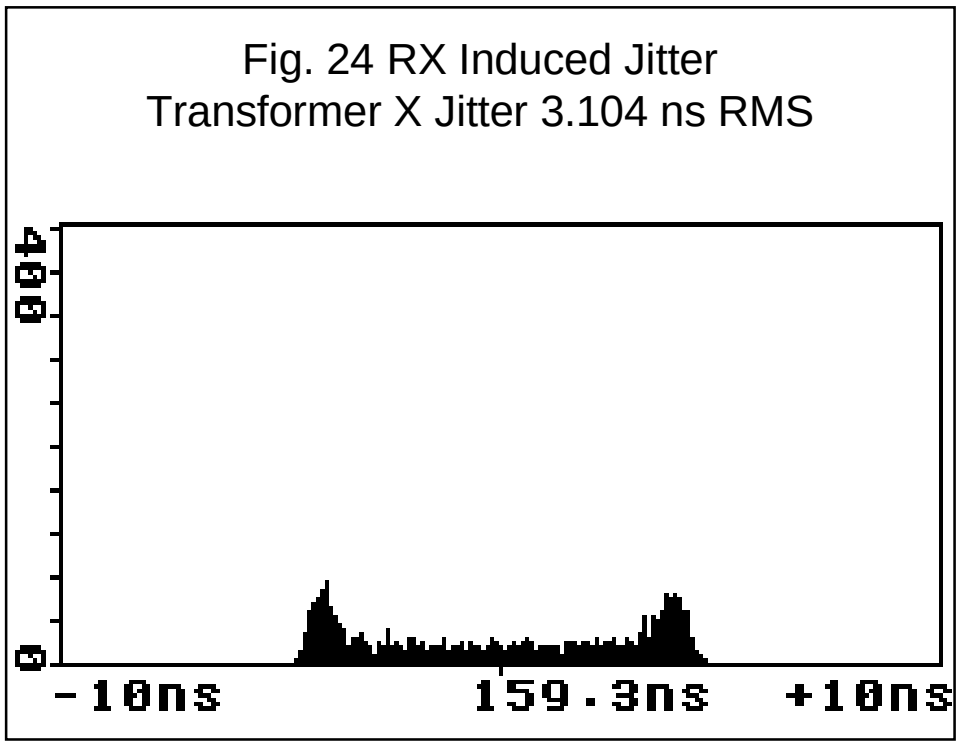


Fig. 24 RX Induced Jitter
Transformer X Jitter 3.104 ns RMS
-10ns
159.3ns
+10ns

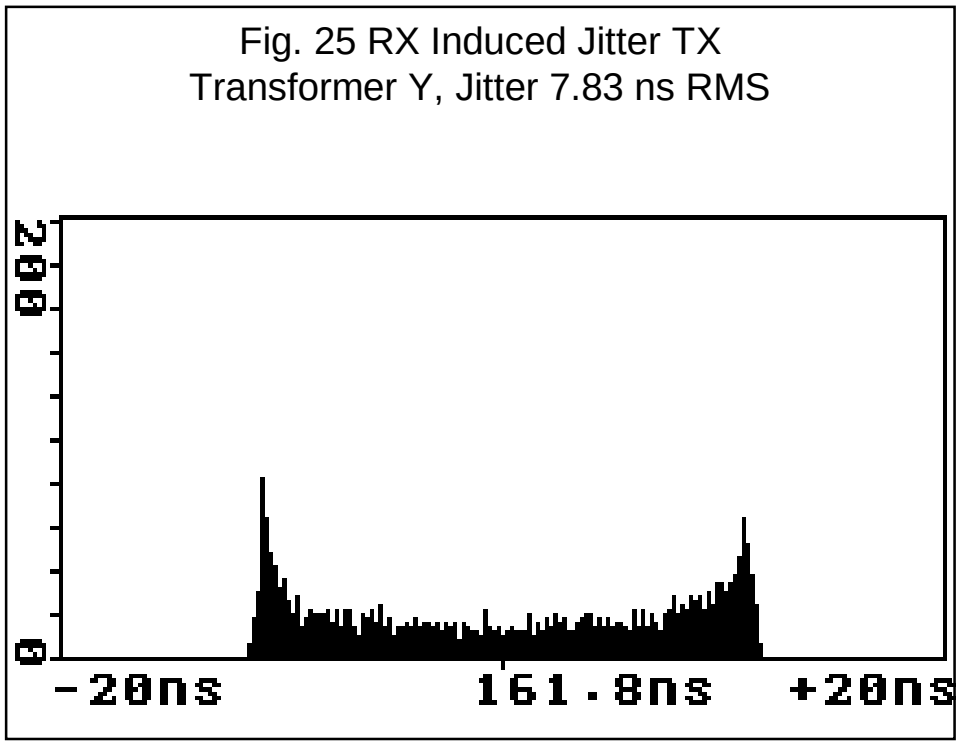


Fig. 25 RX Induced Jitter TX
Transformer Y, Jitter 7.83 ns RMS
802
0
-20ns
161.8ns
+20ns

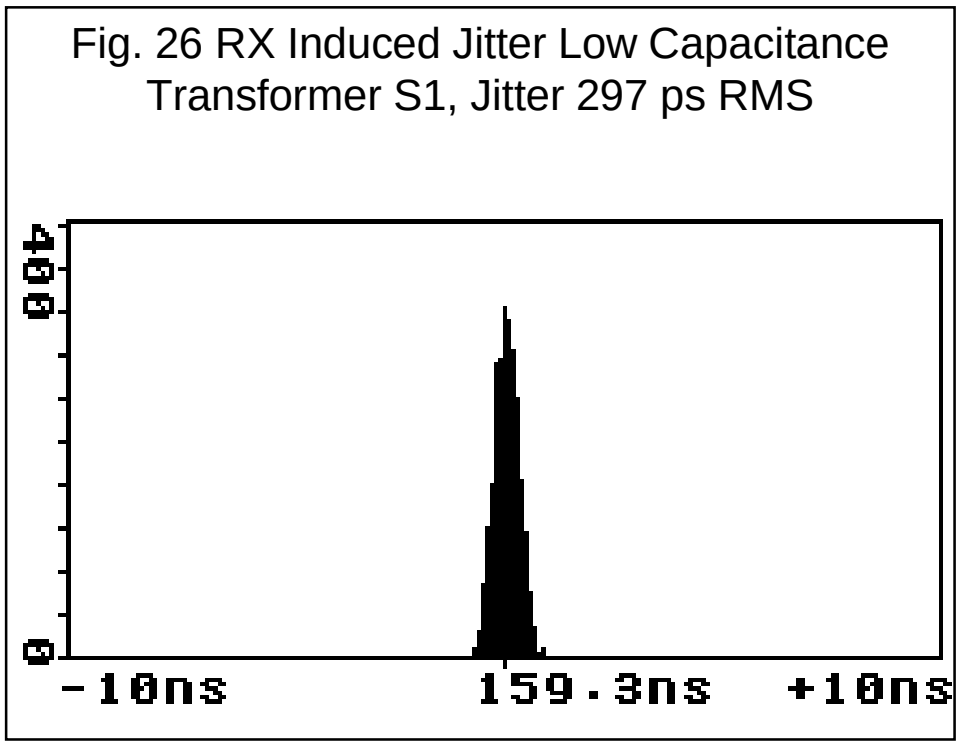


Fig. 26 RX Induced Jitter Low Capacitance
Transformer S1, Jitter 297 ps RMS
804
0
-10ns
159.3ns
+10ns

Fig. 27 TX Induced Jitter No Transformer
Jitter 19.367 ns RMS

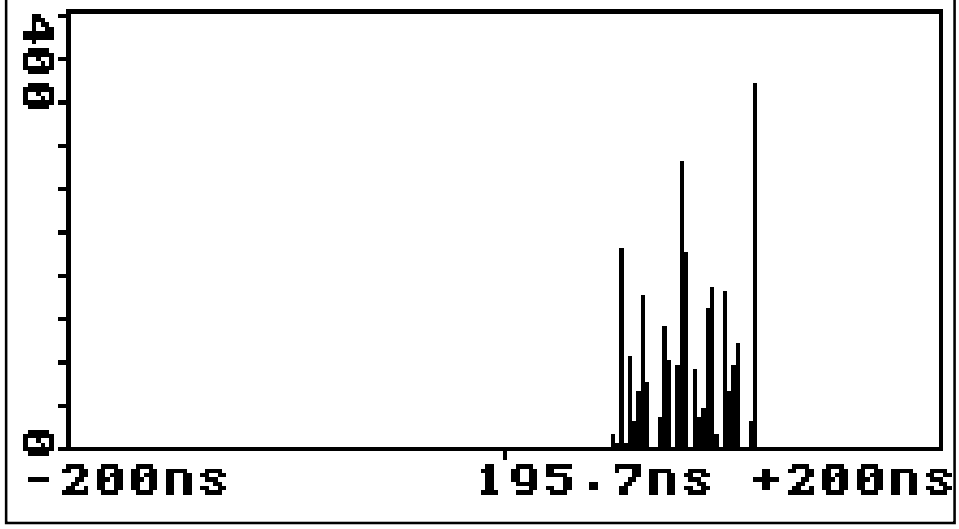


Fig. 28 TX Induced Jitter Hi Capacitance
Transformer X, Jitter 84.5 ns RMS

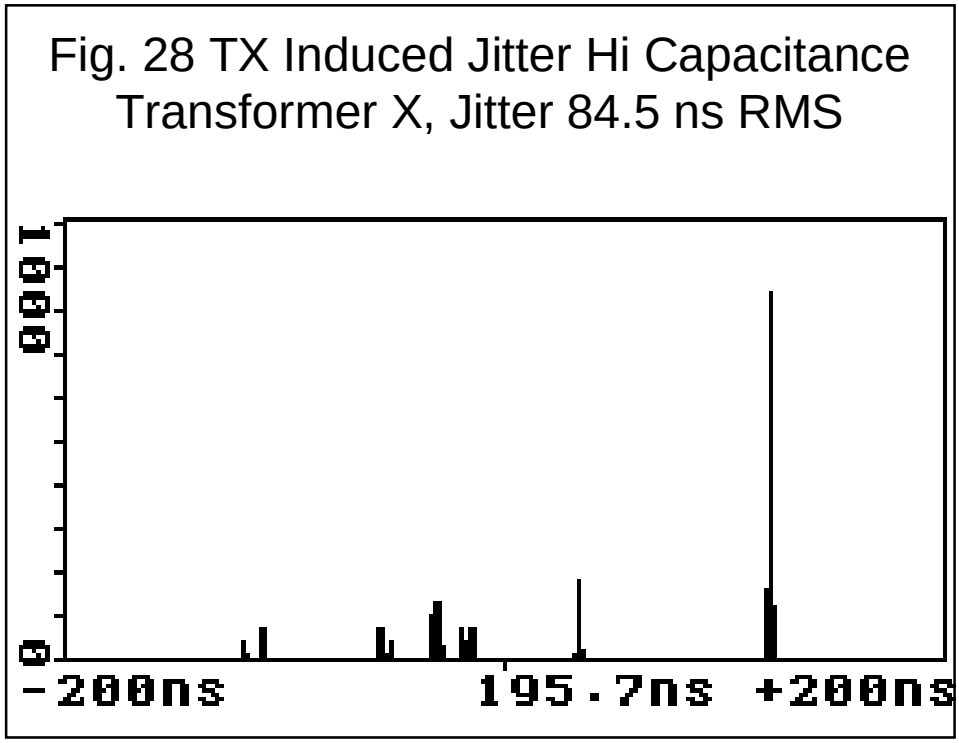


Fig. 29 TX Induced Jitter Lo Capacitance Transformer S1, Jitter 1.64 ns RMS

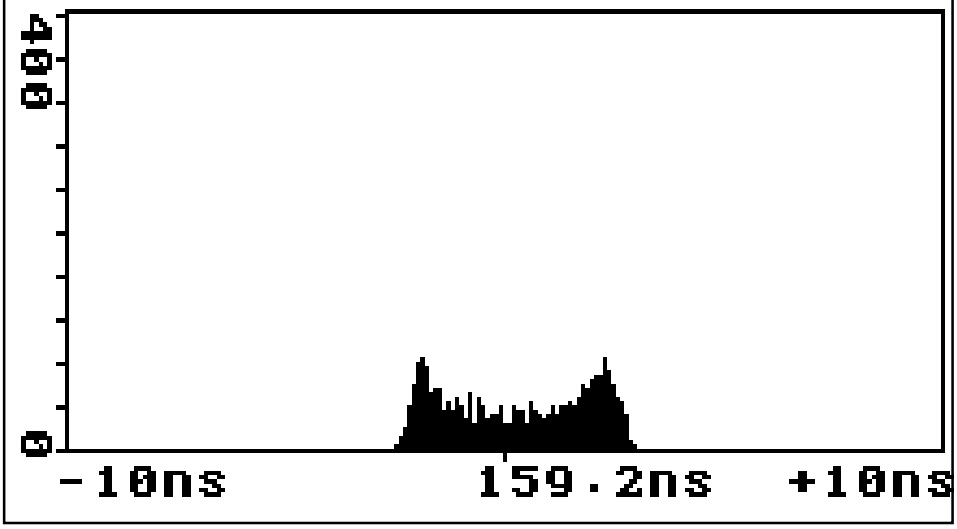


Fig. 30 TX Induced Jitter Shielded Transformer S2, Jitter 302 ps RMS

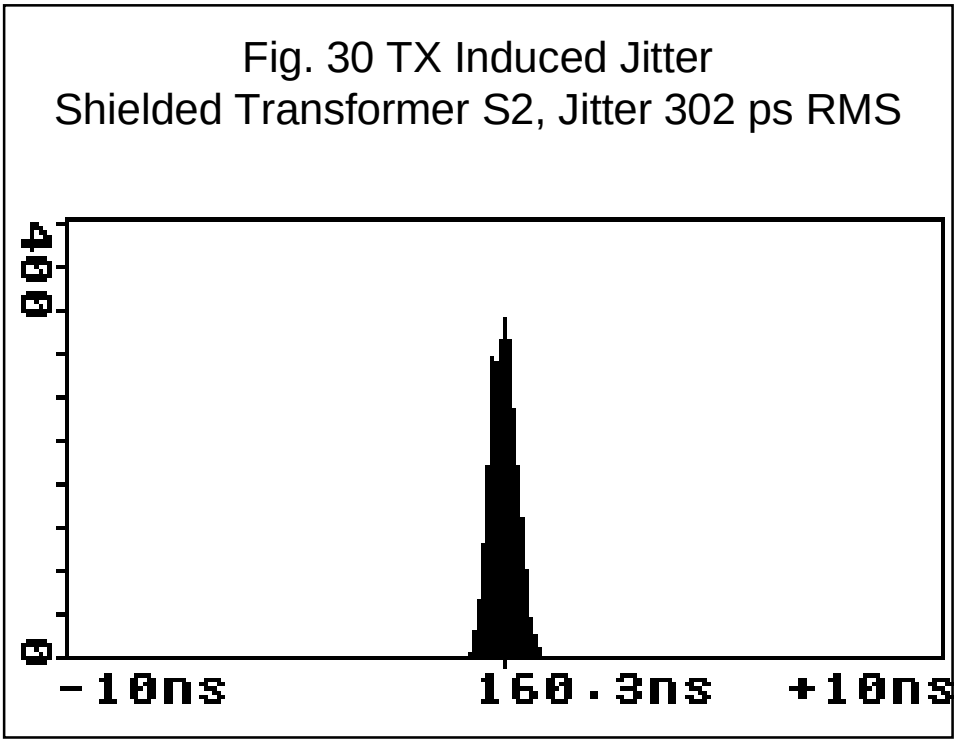
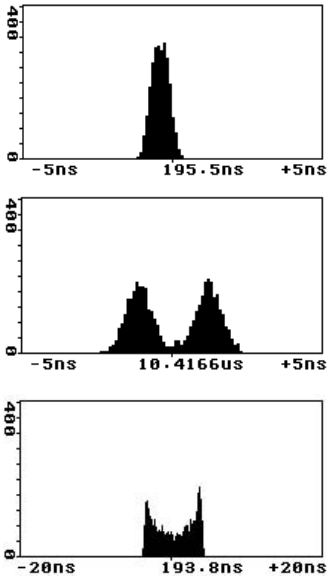


Fig. 31 Jitter Histogram Interpretations

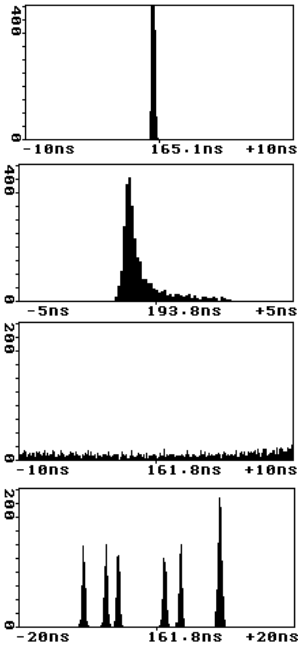


Gaussian Distribution

Bi-value Gaussian

Sine Variation of Period

Fig. 32 Jitter Histogram Interpretations



Narrow Gaussian

(system residual jitter)

Asymmetric Period Variation

White Noise Period

Multiple Discrete Periods

Fig. 33 Reclocking RX with Transformer Isolation

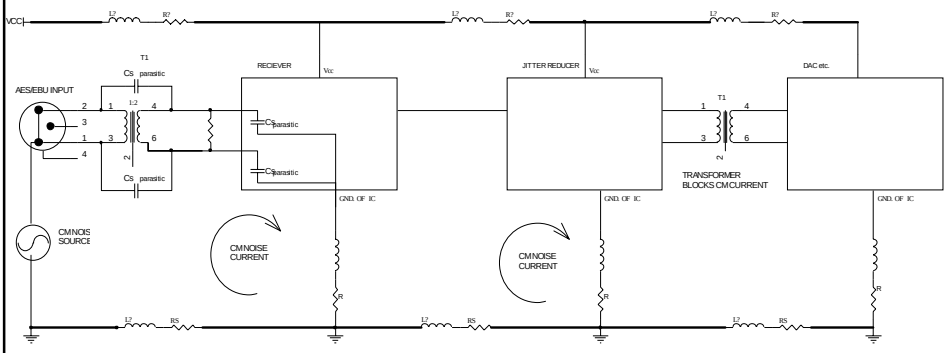


Fig. 34 Balanced Transmission System Using Shielded Transformers

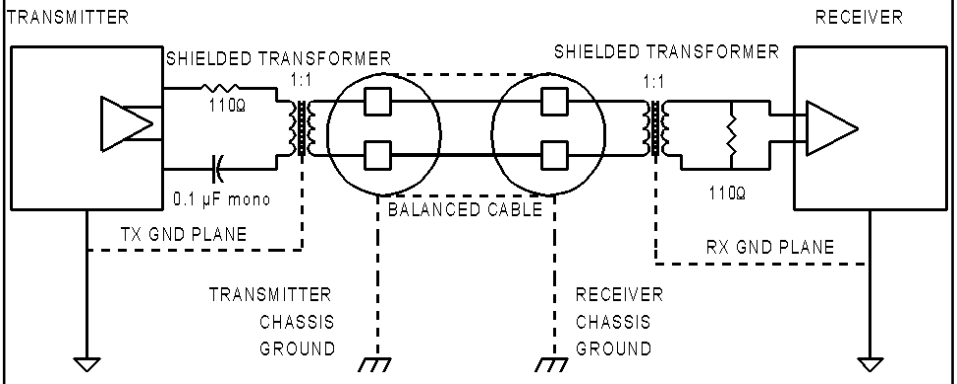


Fig. 35 Application of Transformers to Unbalanced System

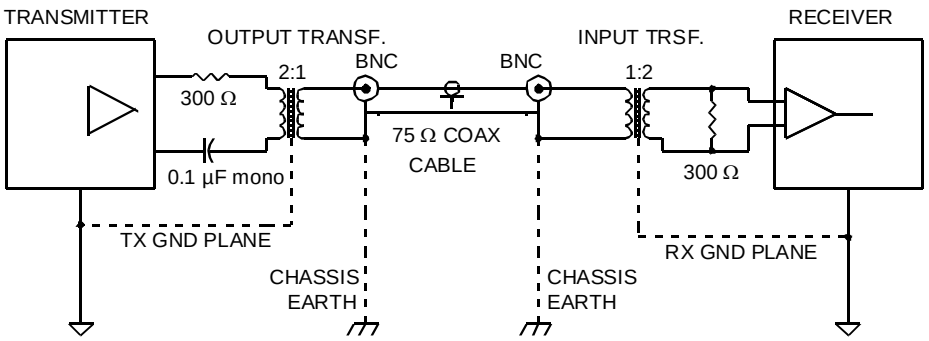
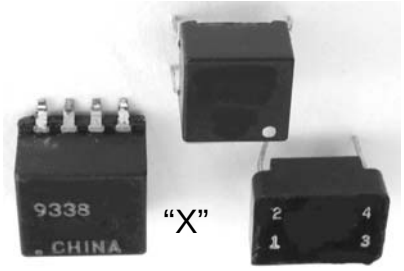


Fig. 36 Transformer Parameter Comparison (* Tested Units)

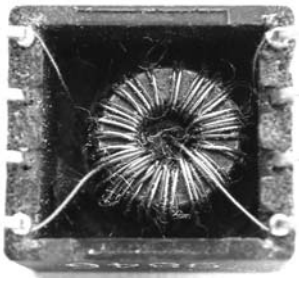
Parameter	Unit	A	B	C	D	E	F	V	X *	Y *	S1 *	S2 *
Primary Inductance	µH	2500	250	2000	3500	900	1522	600 - 2200	2500	225	300	850
Capacitance P - S	pF	25	8	28	23	16	31	5.5	25	9	2.0	3.0
Shielded Cap.	pF							1.5		2		0.5
LF cutoff F_{LOW}	kHz	3.0	26.0	3.0	20.0	6.5	7	24.3	3.0	10	32.0	13.0
HF Cutoff F_{HIGH}	MHz	55	50	55	28	150	80	9	55	40	200	100
RMS Jitter	ps	1950	1260	1900	2400	1320	1250	1060	1950	2902	332	390
CMRR 7.0 MHz 50Ω	dB	23	32.5	21.5	23.5	27	18.9	38	23	37.5	52.0	50.5
Pulse Aberration	%	11	32	20	4	13	11	51	11	20	4	4
Ratio error		3%							3%	22%	1%	1%

Fig. 37 Transformer Construction



"X"

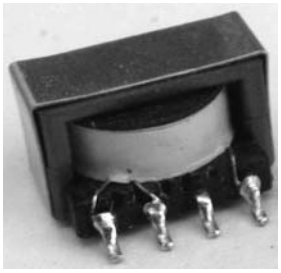
Encapsulated Toroids



Toroid before encapsulation

"Y"

"S1, S2"



Machine Wound, Varnish Dip

Precision wound Bobbin, Clip Assembly

Fig. 38 Improved Receiver Circuits with Shield Beads, CM Choke and Shielded Transformer

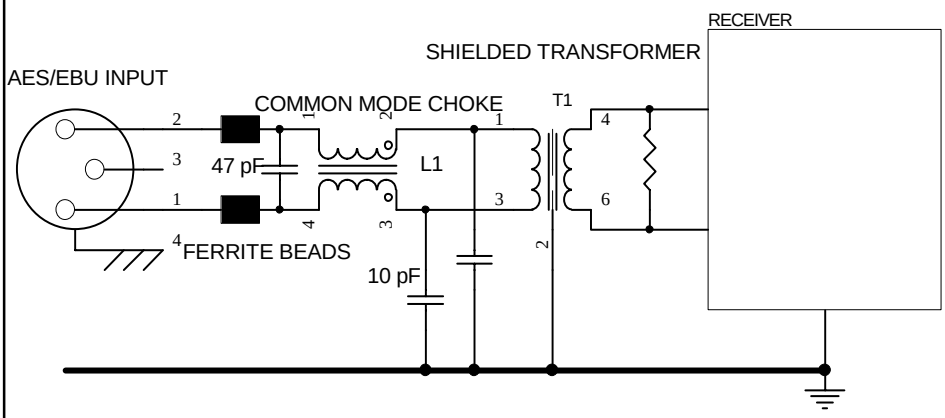
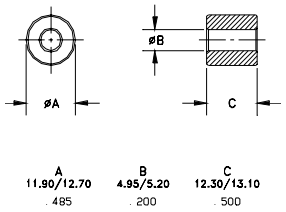
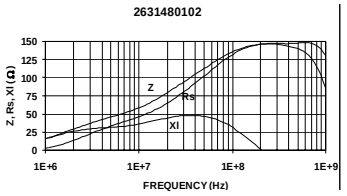


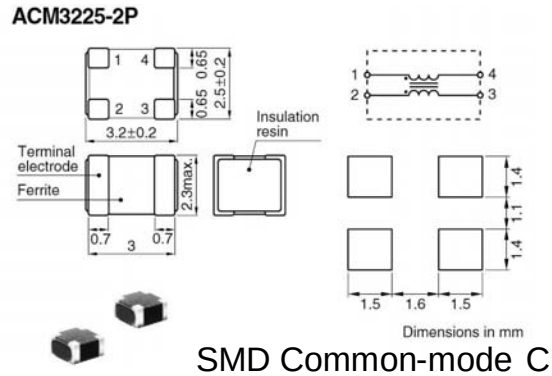
Fig. 39 Common-mode Chokes

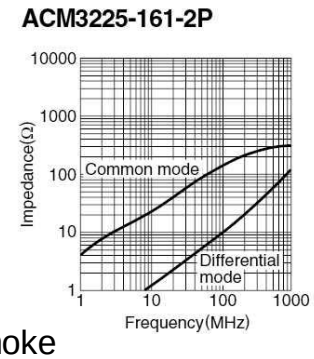
Thru Hole Bead





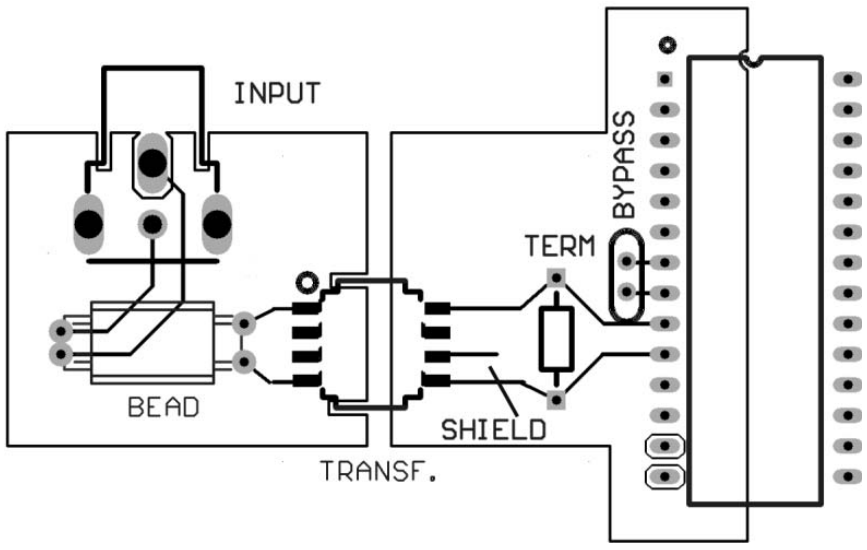
Bead Impedance Per turn





SMD Common-mode Choke

Fig. 40 Suggested PCB Groundplane Layout for Transformer Input Receiver



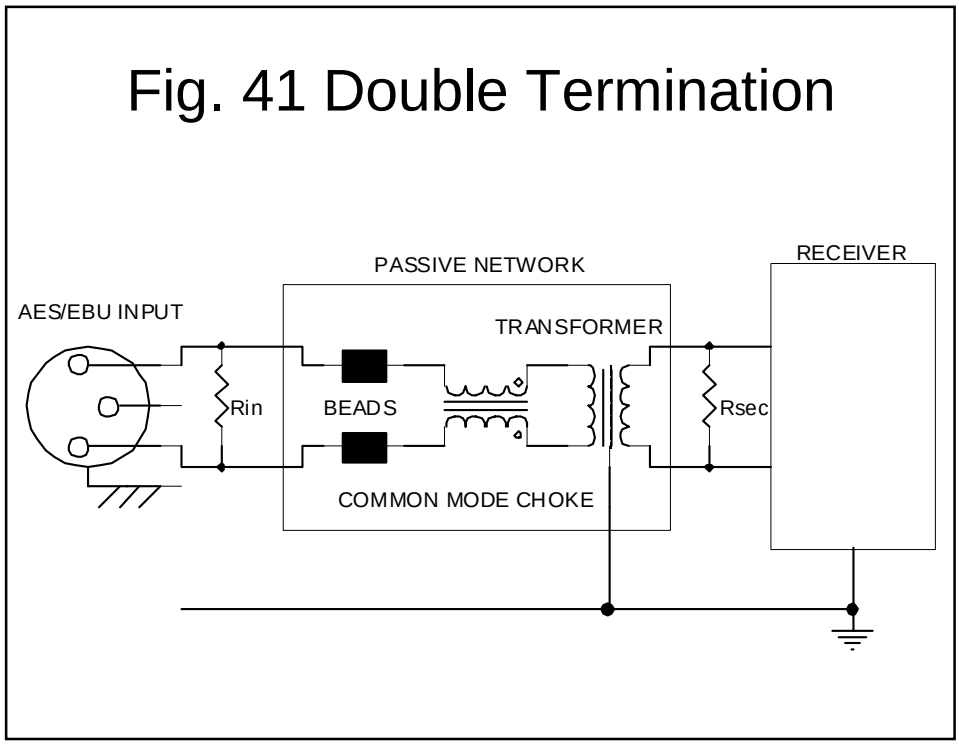


Fig. 41 Double Termination
PASSIVE NETWORK
RECEIVER
AES/EBU INPUT
TRANSFORMER
Rin
BEADS
Rsec
COMMON MODE CHOKE

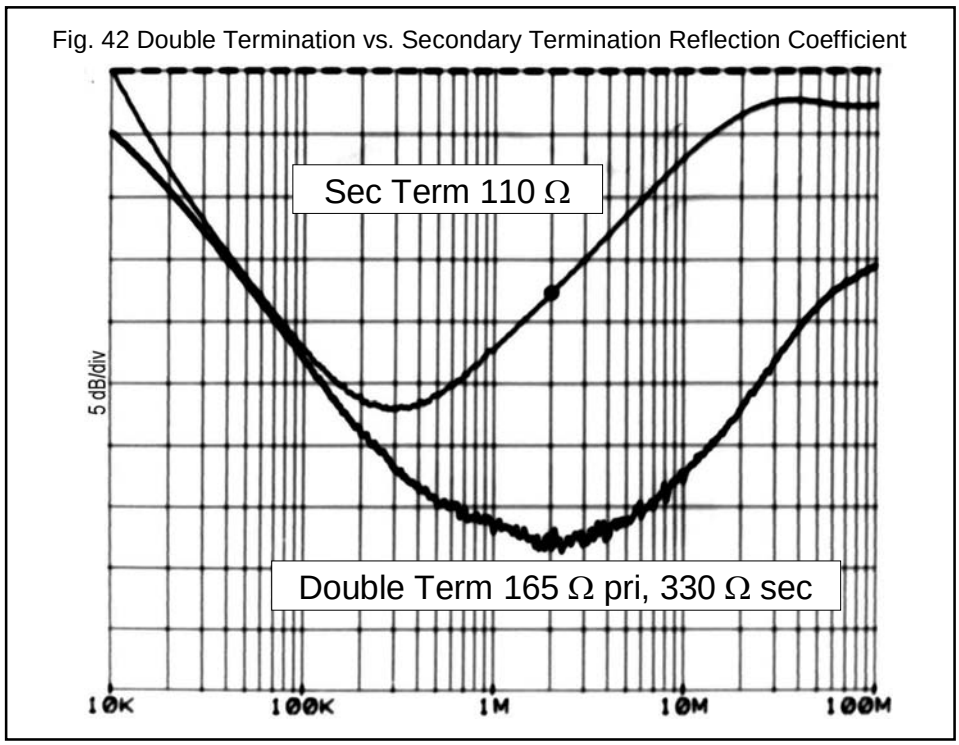


Fig. 42 Double Termination vs. Secondary Termination Reflection Coefficient
Sec Term 110 Ω
5 dB/div
Double Term 165 Ω pri, 330 Ω sec
10K
100K
1M
10M
100M